8. (original): The method according to claim 1, further comprising resetting the repeat flag after executing the target instruction the predetermined number of times.

9. **(currently amended):** A processor including interruptible repeat instruction processing, comprising:

a program memory for storing instructions including a repeat instruction and a target instruction;

a program counter for identifying current instructions for processing;

a loop control unit for executing the repeat instruction to a) store and change a loop count value in a repeat count register and b) prevent an instruction after the target instruction from being fetched until the loop count value reaches or exceeds a predetermined value; and

an execution unit for repeatedly executing the target instruction until the loop count value reaches or crosses the predetermined value;

wherein the executing ~~may be~~ is able to be interrupted during a processing exception to load a first instruction from an interrupt service routine into an instruction register for subsequent execution, the first instruction being determined without reference to a program counter.

claim 10 unchanged See original claim on 06/01/01 D.P. 09/28/04

10. (original): The processor according to claim 9, wherein the repeat instruction itself includes the loop count value.

11. (original): The processor according to claim 9, wherein the repeat instruction includes an address specifying a memory location that includes the loop count value.